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A Low Power SRAM Cell for High Speed Applications Using 90nm Technology

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Abstract: In this paper proposed a novel design of a low power SRAM cell which is used for the high speed operations. The model uses the voltage mode method which is used reducing the voltage swing during the write operation switching activity. The Dynamic power dissipation increases when the operating frequency of SRAM cell increases. In this proposed design we use two voltage sources connected with BL (Bit line) and BAL (Bit bar line) for reducing the voltage swing during the write "1" or write "0" operation. The simulation is done using the LT Spice IV Software in 90nm CMOS technology with 1V Supply Voltage. Dynamic power for different frequencies like 500MHz, 1GHz and 2GHz is calculated. We compare it with the conventional 6-T SRAM cell. The simulation result is shown that the power dissipation is almost constant even the frequency of the proposed SRAM model increases. This justifies the reduction of the dynamic power dissipation for high frequency CMOS VLSI design.
Keywords: CMOS, RAM, ROM, BL, WL, SRA, BLB, VTC.

Introduction

Today, Chip systems are always a fast emerging market. They incorporated increasingly complex functions that require a greater memory capacity. Static random access memory (SRAM) is the most commonly used solution, where bandwidth or low power, or both, are primary considerations. SRAM is a type of semiconductor memory where the static word indicates that, unlike dynamic RAM (DRAM), it does not need to be updated periodically, since SRAM uses a bistable latch circuit to store each bit. The SRAM exhibits data remanence, but remains volatile in the conventional sense that the data is eventually lost when the memory is not turned on. SRAM is also easier to control (interface to) and, in general, more truly random access than modern types of DRAMs.

The growing demand for greater data storage capacity has led the development of manufacturing technology and memory to more compact design rules and, consequently, to higher data storage densities. On-chip memory arrays have become widely used subsystems in many VLSI circuits. The efficiency of the memory array area, i.e., the amount of data bits stored per unit area, is one of the key design criteria that determines the overall storage capacity and, by therefore, the cost of memory per bit.

Advances in embedded memory technology have made large random access memory (DRAM) and random access memory (SRAM) common in the current chip system (SoC). The exchanges between large and small memories have made all sizes practical, allowing the SoC to look more than ever like plate level systems. Large embedded memories provide the SoC with a series of benefits, such as improved bandwidth and significant performance that can only be achieved through the use of integrated technologies. The possibility and success of including integrated DRAM and / or large SRAM blocks in a SoC depends primarily on the manufacturing capacity.

An SRAM cell has three different states in which it can be: sleep when the circuit is idle, read when the data has been requested, and write when the content is updated. SRAM to operate in read mode and write mode must have read and write capability, respectively. Both conditions become difficult to satisfy in advanced technologies because of the high degree of variability in the parameters of the thin CMOS transistor, essentially technologies beyond 45 nm. Increasing the size of the memory makes the degree of reliability difficult to satisfy. This is the first challenge for SRAMs in advanced technology nodes. The high energy consumption in portable electronic devices is a matter of serious concern. Reduced battery life and additional requirements for conditioning and cooling are associated with high energy consumption. Static power dissipation due to standby leakage currents is an important component of total power dissipation. Electronic devices contain different types of which many inactive components represent a significant percentage of the total power dissipation of the system.

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DESIGN TECHNIQUE OF SRAM CELL

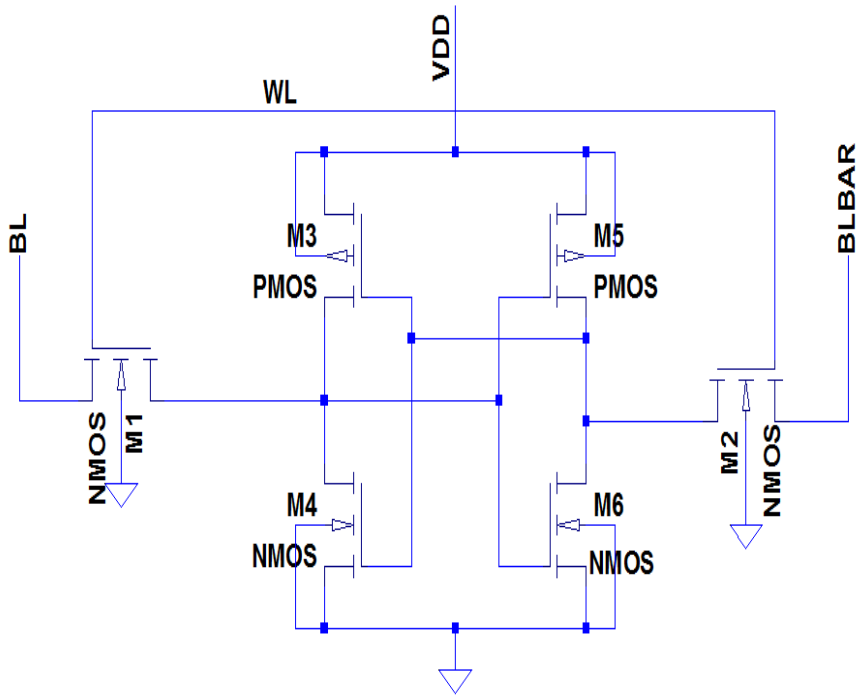

Figure 1 : Basic Circuit Diagram of SRAM Cell

Generally, The actual SRAM architecture based on CMOS inverters is shown in Figure 1. It consists of two back to back connected inverters A and B and two access transistors M1 and M2. The access transistors are connected between inverters and bit lines BL and BLB and their gates are connected to word line WL. The access transistors are turned on through the word line to enable writing and reading operation and turned off during hold condition. Same ports are used for read and write operation. To operate the cell reliably, the sizes of the transistors should be properly designed.

An SRAM cell can store a data bit. A SRAM cell comprises two inverters connected one behind the other that forms a latch and two access transistors. The access transistors are used to write and read access to the cell. An SRAM cell provides the following basic properties:

- Retention: An SRAM cell can retain the data indefinitely while it is activated.
- Read: A SRAM cell can communicate its data. This operation does not affect the data, that is, the reading operation is not destructive.
- Write: The data of an SRAM cell can be set to any binary value, regardless of its original data.

Several topologies of SRAM cells have been reported in the last decade. Among these topologies, the cell of four resistive load transistors (4T), the 4T cell without load and the SRAM cell of six transistors (6T) have received attention in practice, due to their symmetry when storing logic 'one' and logical 'zero'. [4]. Data retention in 4T SRAM cells is guaranteed by the leakage current of the access transistors. Therefore, they are not suitable candidates for low power applications. On the other hand, the data stability in a 6T SRAM cell is independent of the leakage current. In addition, the 6T configuration exhibits a significantly greater tolerance to noise, which is an important benefit especially in scale technologies where noise margins are reduced. That is the main reason for the popularity of the 6T SRAM cell in low power SRAM units instead of the 4T configurations. A 6T SRAM cell consists of two cross-coupled CMOS inverters and two access transistors. The output (input) of the inverters constructs the internal nodes of the cell. Once active, the access transistors facilitate the communication of the internal nodes of the cell with the input / output ports of the cell. The input / output ports of the cell are called bit lines (BL and BLBAR). Bit lines are a means of data communication shared between cells in the same column in an array of cells. Consequently, they have a high capacitive load. The read and write operations are performed through the bit lines as we will see in the next sections.

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PROPOSED SRAM CELL

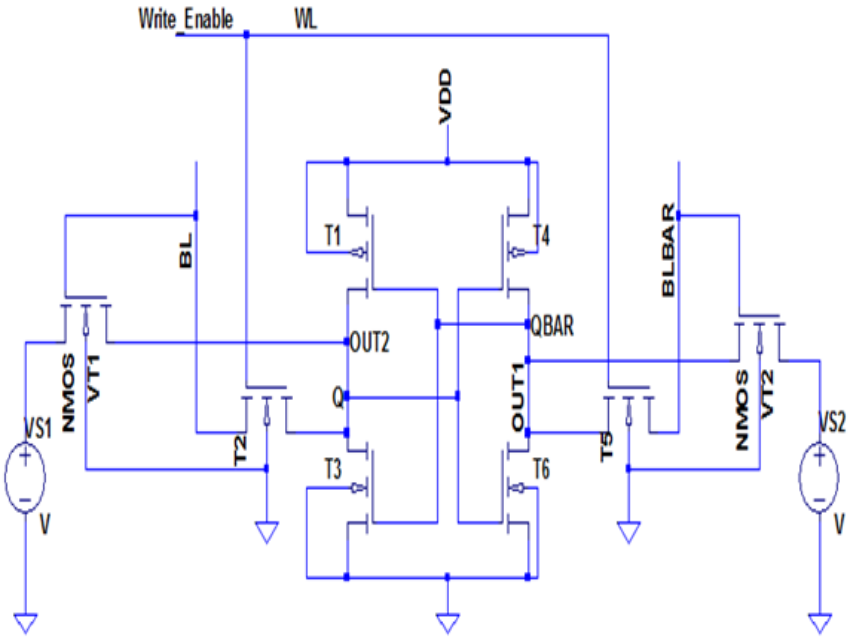

Figure 2 : Proposed SRAM Cell

The schematic of proposed SRAM cell is designed and implemented by using LT SPICE IV. For simulation we are using 1V power supply for different frequencies. VS1 and VS2 have been taken 0.5 volt during simulation. These simulated results are compared with the conventional 6T SRAM cell.

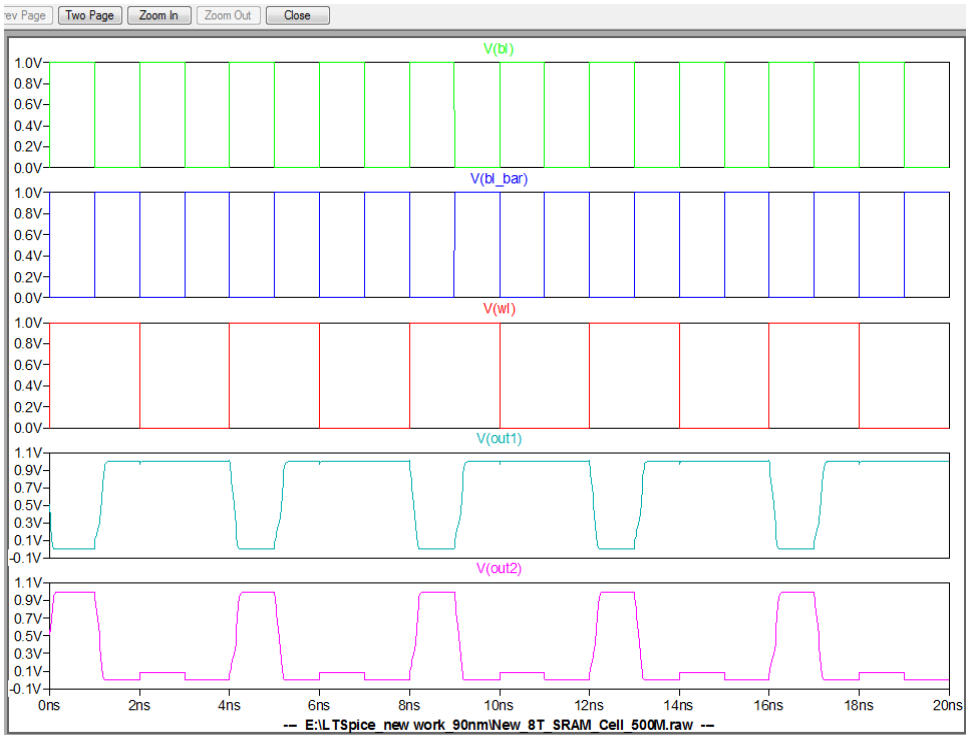

Figure 3 : Proposed SRAM Cell for 500 MHz

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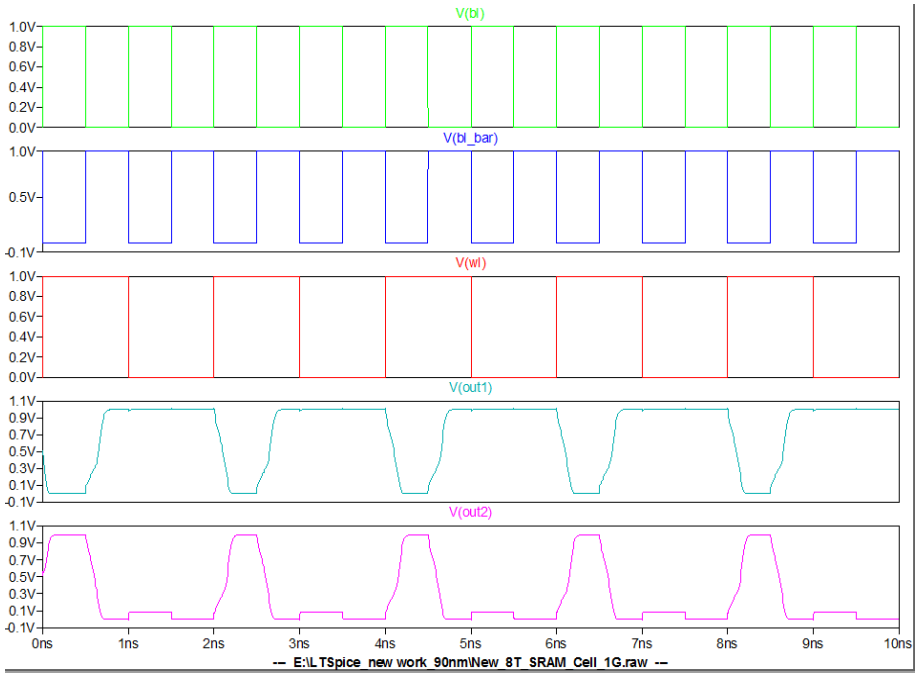

Figure 4 : Proposed SRAM Cell for 1GHz

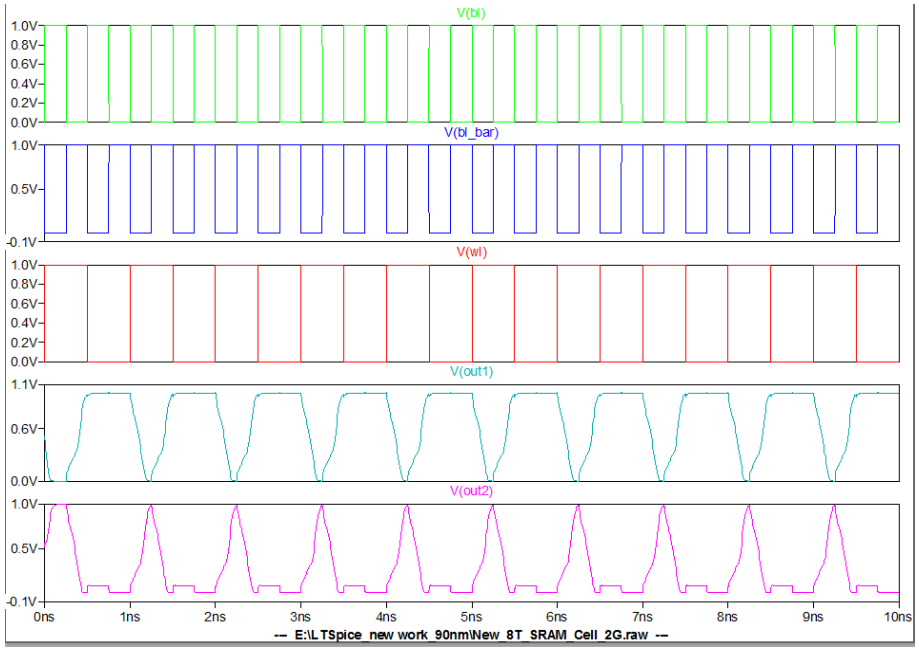

Figure 5 : Proposed SRAM Cell for 2GHz

We simulate the proposed SRAM cell at frequencies of 500 MHz, 1 GHz and 2 GHz, respectively. The simulated results for 500 MHz and 1 GHz were shown in Figures 3 and 4, respectively. In Figures 3-4, it is clear that the loading and unloading time of the bit lines and bitbars improves for a higher operating frequency.

Finally, we calculated the power dissipation in the proposed 500 MHz, 1 GHz and 2 GHz SRAM cell and compared these results with those of the conventional 6 cell SRAM. The width and length used in the proposed model were given in Table 1. The proposed model was simulated in 90nm CMOS technology and that is why we selected the 90 nm length of all transistors. The comparison of power dissipation between conventional SRAM and the proposed model is shown in Table 2.

This shows that if we double the operating frequency of the conventional SRAM cell, the power dissipation is almost double, but in the case of the proposed SRAM energy, the power dissipation at different frequencies is approximately half and almost constant in comparison with the conventional SRAM cell. Therefore, from these results, it is clear that the proposed approach for CMOS-based SRAM design is suitable for high speed VLSI design.

TABLE 1 : Width and length used in the proposed model for Simulation

Transistors	Widths(nm)
T1	175
T2	115
T3	500
T4	175
T5	115
T6	500
VT1	300
VT2	300

TABLE 2 : Comparison of Power Dissipation between the New Design Cell Vs Conventional SRAM Cell

Operating frequency	Power Dissipation in 6T SRAM cell (µW)	Power Dissipation in Proposed SRAM cell (nW)
500MHz	4.890	606.519
1GHz	8.002	606.519
2GHz	11.979	606.519

In the proposed SRAM cell, the crosstalk voltage values increase for one bit, line line (WL) and for outputs compared to the conventional SRAM cell, but these values can be controlled with the help of the width size (W) and length (L) of the transistor.

Conclusion

There are two main types of power dissipation in which dynamic power dissipation has become a major problem in high-speed VLSI designs. In this document we present a new design for the low power dynamic SRAM cell using the voltage mode method. This proposed SRAM cell has two voltage sources that are used to decrease the voltage oscillation at the output during the switching activity. The decrease of the consequences of voltage oscillation in the reduction of the dynamic power dissipation. The dynamic power dissipation for the proposed new SRAM cell is almost stable for high speed operations. Since the number of transistors and the area are raised compared to the conventional 6AM SRAM cell, this drawback can easily be overcome by the low power dissipation even at a very high frequency. This proposed new SRAM cell can be used to make a low-power solution available in high-speed devices such as laptops, smart phones, programmable logic devices, etc.

References

[1]. A. P. Chandrakasan and R. W. Broderson, "Minimizing powerconsumption in digital CMOS circuits," Proc. of the IEEE, vol. 83,no.4, pp. 498-523, April 1995.G Tuangzhi Dai and Tiequn Chen. " Design on measurement and control system of cleaning robot based on sensor array detetion", In IEEE International conference on control automation Guangzhou, CHINA-MAY 30 to June 1, 2007.

[2]. Gu Ming, Yang Jun, Xue Jun, "Low power SRAM design using charge sharing technique," 6th International Conference On ASIC, ASICON, pp.19-23, Oct.2005.

[3]. B. Amrutur and M. Horowitz, "Speed and power scaling of SRAM's," IEEE J. Solid-State Circuits, vol. 35, no. 2, pp. 175–185, Feb. 2000.

[4]. I. Thoidis, D. Sourdris, I. Karafyllidis, A. Thanailakis, and T. Stoursitis, "Design Methodology of Multiple-Valued Logic Voltage-Mode Storage Circuits", IEEE Internatinal Symposium on Circuit and System, pp. 125-128, March 1998.

[5]. Tae-Hyoung Kim, Jason Liu, John Keane, Chris H. Kim;" A High-Density Subthreshold SRAM with Data-Independent Bit line Leakage and Virtual Ground Replica Scheme" Proc. of International Solid State Circuits Conference, pp. 330-331, February 2007.

[6]. Naveen Verma, Anantha P. Chandrakasan, "A 65nm 8T Sub-Vt SRAM Employing Sense-Amplifier Redundancy" Proc. Of International Solid State Circuits Conference, pp. 328-329, February 2007.

[7]. Bo Zhai, David Blaauw, Dennis Sylvester, Scott Hanson "A Sub-200mV 6T SRAM in 130nm CMOS" Proc. Of International Solid State Circuits Conference, pp. 332-333, February 2007.

[8]. Loveneet Mishra, Sampath Kumar and Sangeeta Mangesh, "Design and implementation of low power SRAM structure using nanometer scale" , International Conference on Advances in Electrical, Electronics, IEEE, Information, Communication and Bio-Informatics (AEEICB16), 2016.

[9]. Prashant Upadhyay, R. Kar, D. Mandal and S. P. Ghoshal, "A Low Power CMOS Voltage Mode SRAM Cell for High Speed VLSI Design", Asia Pacific Conference on Postgraduate Research in Microelectronics & Electronics (PRIMEASIA), pp-25-29, 2012.